PATENT ABSTRACTS OF JAPAN

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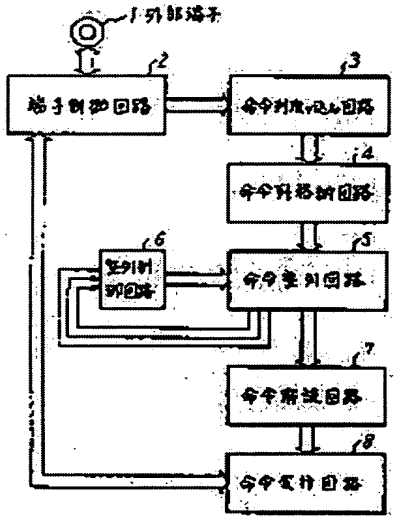
(54) INFORMATION PROCESSOR



(57)Abstract:

PURPOSE: To shorten the decoding time of an instruction word and to reduce the hardware quantity of an instruction decoding circuit by providing the display of a binary number at a part of the instruction word to show the length of this instruction word.

CONSTITUTION: An instruction aligning circuit 5 performs the program searching of an instruction for an instruction decoding circuit 7 to decode the corresponding instruction. In this case, the head position of each instruction is designated in an instruction train. At the same time, the head position of each instruction is also designated by an alignment control circuit 6. The circuit 6 adds the length of instructions aligned at present to the head positions of instruction aligned at present to decide the head position of a new instruction. Then the head three bits of the instructions aligned by the circuit 5 are used as the length of the instructions aligned at present. In other words, the byte length of each instruction word is shown in a binary number of three digits with use of bits 2 – 0. Thus it is not required to use the circuit 7 for detection of the instruction word length in an information processor.

LEGAL STATUS

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